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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/048,207	01/28/2002	Lars-Peter Heineck	P02,0022	4793

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EXAMINER	
LATTIN, CHRISTOPHER W	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/048,207	HEINECK ET AL.	
	Examiner	Art Unit	
	Christopher W Lattin	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 9-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 9-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 January 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention for the reasons set forth below.

Claim 9 line 8 requires that the sacrificial layer be formed before ALL spacers in the first region, yet the specification repeatedly teaches that spacer structures are already present on the structures. It is therefore unclear what applicant regards as the invention: that no spacers are formed prior to the sacrificial layer or that at least one more spacer layer will be formed after forming the sacrificial layer.

Furthermore line 8 of claim 9 limits the invention to "forming sacrificial contacts in the second region before all spacers are formed in the first region". It is unclear what applicant intendeds to be formed in the first region: sacrificial contacts or spacers.

Finally, the term "two spacers" in line 6 of claim 9 could refer to either spacers formed from one layer, but on two sides of the gate (i.e. spacers twelve) or two spacer layers (i.e. spacers 12 and 13).

With reference to claim 13, "a dopant having different conductive types" renders the claim indefinite. It is unclear how one dopant could have different conductive types.

Appropriate correction or clarification of these claims is required.

For purposes of examination the claims will be read in accordance with the specification, particularly Figures 13-18. Therefore the term "all" will be interpreted as indicating that the sacrificial layer is formed prior to at least one of the spacer layers. The claim will also be interpreted to indicate spacers in a first region and a sacrificial contact in the second region. Lastly, it will be assumed that the applicant intended to form more than one spacer layer. In the event that applicant intended to claim two layers of spacers, further clarification is required in claim 10 regarding to which spacer the claim refers.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Inaba et al. (U.S. Patent 6,153,476).

Inaba et al. teach a method for producing an integrated semiconductor component comprising the steps of preparing a semiconductor substrate 11 having at least one first region 11b and at least one second region 11a; producing gate paths 21B

in the first region and the second region of the semiconductor substrate 11; producing source/drain regions 25B neighboring the gate paths in the first region of the semiconductor substrate; forming at least two spacers 22a 22b on gate paths 21B in the first region; producing source/drain regions 25A neighboring the gate paths in the second region of the semiconductor substrate; forming sacrificial contacts 62 in the second region before all spacers are formed in the first region (See Figure 4A); and preparing contacts 33 to predetermined source/drain regions in the second region and the first region, wherein the spacers are formed of a material selected from a group consisting of silicon oxide, silicon nitride and oxynitride.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba et al. (U.S. Patent 6,153,476) in view of Naito et al. (U.S. Patent 5,856,219, cited by applicant).

Inaba et al. teach a method for producing an integrated semiconductor component comprising the steps of preparing a semiconductor substrate 11 having at least one first region 11b and at least one second region 11a; producing gate paths 21B in the first region and the second region of the semiconductor substrate 11 by applying

a gate material layer 21 on the semiconductor substrate, providing a protective layer 26 selected from a group consisting of silicon nitride, silicon oxide and oxynitride layers on the gate material layer 21 and then structuring the gate material layer 21 and protective layer 26 to form the gate path; producing source/drain regions 25B neighboring the gate paths in the first region of the semiconductor substrate; forming at least two spacers 22a and 22b on gate paths 21B in the first region; producing source/drain regions 25A neighboring the gate paths in the second region of the semiconductor substrate; forming sacrificial contacts 62 in the second region before all spacers are formed in the first region (See Figure 4A); and preparing contacts 33 to predetermined source/drain regions in the second region and the first region, wherein the spacers are formed of a material selected from a group consisting of silicon oxide, silicon nitride and oxynitride, but fails to teach that the gate is comprised of polysilicon. Naito et al. teach forming a gate path of polysilicon. It would have been obvious to one skilled in the art at the time of the invention to utilize polysilicon as taught by Naito et al. as the "gate materials" referenced in column 7 of Inaba et al. in order to form a gate with low resistance.

Claims 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba et al. (U.S. Patent 6,153,476) in view of Naito et al. (U.S. Patent 5,856,219) as applied to claim 11 above and further in view of Moslehi (U.S. Patent 5,322,809).

Inaba et al. in view of Naito et al. are applied supra and teach all of the limitations of claims 12 and 13, but fail to specifically teach that the protective layer is formed with a thickness so that the protective layer exhibits a thickness of less than 100nm after the

structuring step or that after the step of forming sacrificial contacts and prior to the step of preparing contacts to the predetermined source/drain regions, removing the protective layer from the gate, paths, at least in the first region, and then doping the gate paths in the first region with a dopant having different conductive types and forming silicides on the gate paths. Moslehi teaches the formation of a protective layer 24 of 20-100 nm and removing the layer to later form a silicide on the doped gate paths of $CoSi_2$, $TaSi_2$, $TiSi_2$ and WSi_X. It would have been obvious to one skilled in the art at the time of the invention to use a protective layer of 20-100 nm to protect the gate with a minimal amount of material, thus saving time and money. It further would have been obvious to dope the gate and replace the protective layer of Inaba et al. with a silicide layer taught by Moslehi in order to reduce the contact resistance of the gate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Lattin whose telephone number is (703) 305-3017. The examiner can normally be reached Monday through Friday from 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached at (703) 308-3325. The fax numbers for this Group are (703) 872-9318 for responses to non-final actions and (703) 872-9319 responses to final actions.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

CWL
June 12, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800